A 15 GHz Single-Stage GaAs Dual-Gate FET Monolithic Analog Frequency Divider with Reduced Input Threshold Power

KUNIHIKO KANAZAWA, MASAHIRO HAGIO, MASARU KAZUMURA, AND GOTA KANO

Abstract—**A 15 GHz single-stage GaAs dual-gate FET monolithic analog frequency divider with a reduced input threshold power has been designed and fabricated. Use of the dual-gate structure for the FET mixer contributed to a simplified circuit configuration. Introduction of the rejection filter at the output port resulted in a reduction of the input threshold power to 1.4 dBm.**

I. Introduction

FREQUENCY DIVISION is the subject of increasing interest in the field of microwave communication systems, especially in phase-locked loops (PLL's). There have been two categories of frequency-dividing circuits. The first comprises logic circuits which contain digital static and digital dynamic dividers. Although they are capable of very low turn-on threshold input power performance, these circuits need very high performance FET's for the microwave frequency range. The second category, which contains analog frequency-dividing circuits, does not require FET's with such high performance because the analog frequency divider is inherently suitable for high-frequency operation, the only limitation being the gate delay times for the subharmonic frequency. The regenerative type of analog frequency divider [1]–[3] is attractive for the ease it affords in circuit design. Monolithic regenerative analog frequency dividers have been lately reported [4]–[6].

Fig. 1 shows a diagram of a regenerative analog frequency divider composed of a mixer, a bandpass filter, amplifiers, and a feedback circuit. The basic operation is as follows. A signal component at the subharmonic of the input signal frequency is present initially, coming either from noise or from input signal transients. The subharmonic signal is mixed with the input signal to again produce the subharmonic signal, which is subsequently filtered out and regenerated in the loop. The saturated subharmonic signal power, where the mixing gain is equal to the feedback loop loss, can be taken out at the output port.

Although the analog frequency divider provides well-behaved high-frequency divider performance, it possesses two substantial drawbacks. One is the complex circuit configuration needed because of poor separation of the signals [1], [4]. The other is its undesirably high input threshold power [4], [5]. The purpose of this work is to resolve these issues by using the dual-gate structure for the FET mixer and the rejection filter at the output port. The dual-gate FET and the rejection filter are useful for improving the isolation of the signals and for increasing the conversion gain, respectively [7]. The dual-gate FET simplifies the circuit configuration. The rejection filter is effective for reducing the input threshold power. This paper describes work undertaken to design, fabricate, and test a 15 GHz single-stage GaAs dual-gate FET monolithic analog frequency divider with reduced input threshold power.

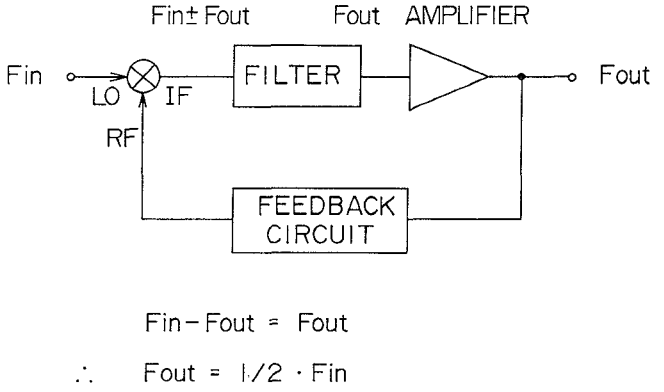

Fig. 1. Block diagram of the regenerative analog frequency divider.

II. Design

For the purpose of achieving a simple circuit configuration, a dual-gate FET suitable for avoiding cumbersome passive couplers is utilized as the mixing element. This dual-gate FET mixer is designed to have such a high gain [8], [9] that the amplifiers in the loop in Fig. 1 can be removed. As a result, a single stage analog frequency divider can be achieved by use of the dual-gate FET mixer [3].

An equivalent circuit of the designed single stage dual-gate FET analog 1/2 frequency divider is shown in Fig. 2. The divider is composed of the FET mixer, the input matching circuit, the feedback circuit, and the bias circuit. The input signal is applied to the second gate and

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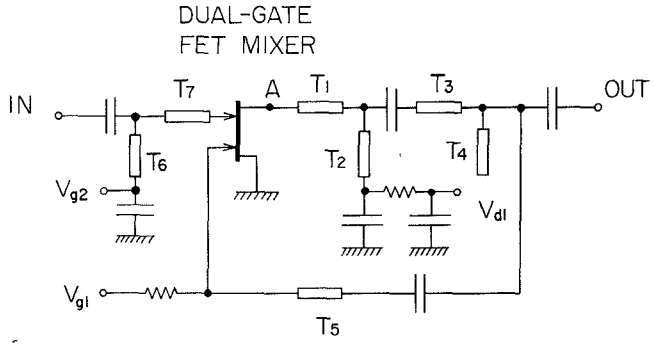

Fig. 2. Equivalent circuit of the single stage dual-gate FET analog 1/2 frequency divider.

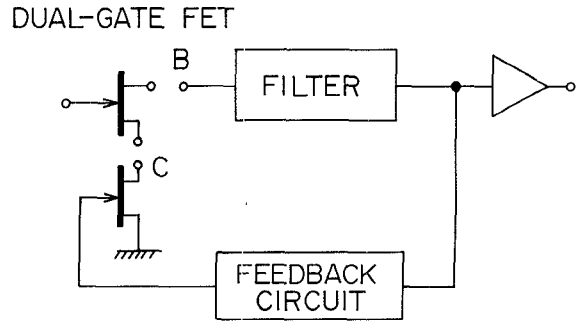

Fig. 3. Block diagram of the open-loop circuit.

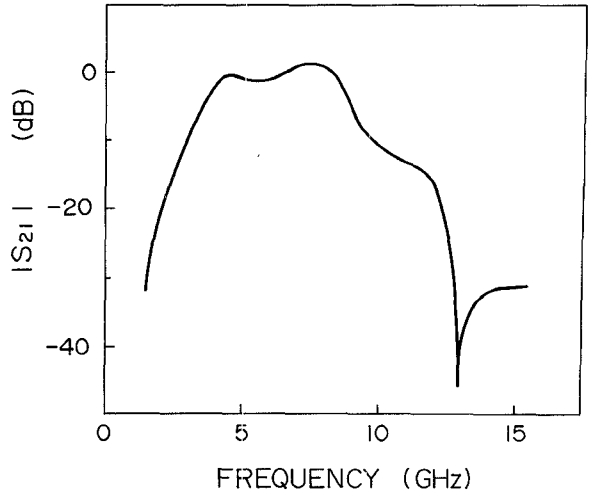

Fig. 4. Simulated $|S21|$ of the open-loop circuit as a function of frequency.

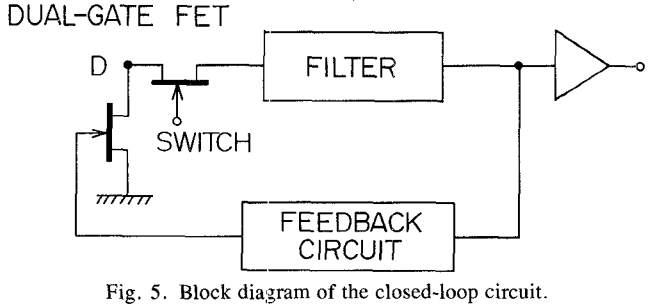

Fig. 5. Block diagram of the closed-loop circuit.

the output signal is driven to the drain port. The feedback circuit returns a part of the output subharmonic signal to the first gate.

The following three techniques are used for reducing the input threshold power:

1) rejection of the input frequency signal at the drain port of the dual-gate FET;
2) minimization of the loss of the input matching circuit;
3) optimization of the geometric parameters of the dual-gate FET.

In the first technique, the rejection of the input frequency signal at the drain port of the dual-gate FET is achieved by using the rejection filter. As a result, the input threshold power is reduced because the rejection of the input frequency signal results in an increase in the conversion gain of the dual-gate FET mixer by returning the LO signal to the mixer output port [7]. It is noted that a very compact spiral open stub and a drain bias circuit containing a microstrip line are used to provide the short circuit at the drain port as the rejection filter. In the second technique, the minimization of the loss of the input matching circuit is performed by a computer simulation of the matching circuit composed of two microstrip lines using the large-signal scattering parameters of the dual-gate FET. In the third technique, the optimization of the FET parameters is also carried out by a computer simulation. The optimized FET parameter is the gate width, which is 300 μm for obtaining a high mixing conversion gain for a gate length of 0.7 μm.

For the purpose of achieving the analog divider operation, two computer simulations are effectively performed for the feedback circuit. One simulation is done for the suppression of the loop loss for the subharmonic band of the input signal frequency under the condition giving the short circuit at point A in Fig. 2. The scattering parameter $|S21|$ from B to C in Fig. 3, which shows the open-loop circuit, is designed to have a maximum value at the subharmonic band. The simulated scattering parameter $|S21|$ is shown in Fig. 4. The designed input operation frequency band ranges from 13 to 15 GHz.

The other simulation is done in order to realize the effective divider operation by using the design technique of the oscillation. The effective divider operation is achieved under the condition where the oscillation can be easily accomplished by changing the gate bias from a value slightly below I_{dss} to a value of near pinchoff. The scattering parameter $|S11|$ at point D in Fig. 5, which shows the closed-loop circuit containing a switch [5], [8], is designed to have a value larger than 1.0 at the subharmonic band of the input signal frequency for the bias of the oscillation. The simulated scattering parameter $|S11|$ is shown in Fig. 6. The resultant optimized parameters are summarized in Table I. It is noteworthy that all additional oscillations are suppressed in the analog frequency divider operation by biasing the gate slightly above pinchoff, where the dual-gate FET provides the high conversion gain.

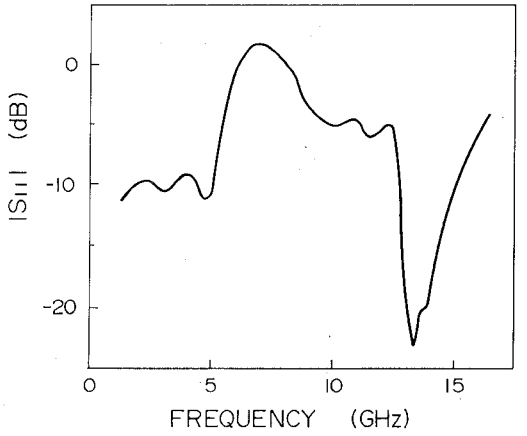

Fig. 6. Simulated $|S11|$ of the closed-loop circuit as a function of the frequency for the bias of the oscillation.

TABLE I
RESULTANT OPTIMIZED PARAMETERS OF THE CIRCUIT

MICROSTRIP LINES	CHARACTERISTIC IMPEDANCE	ELECTRICAL LENGTH
T_1	105 Ω	229°
T_2	105 Ω	81°
T_3	105 Ω	13°
T_4	105 Ω	96°
T_5	105 Ω	153.5°
T_6	89 Ω	35°
T_7	89 Ω	16°

III. FABRICATION

The process used was the full-ion implantation process, local area through-oxide implantation technology (LATIT) [10]. Fig. 7 shows a cross-sectional drawing of the dual-gate FET. The feature of this process is that the surface n^+ layer on the active layer and the deep n^+ layer at the source/drain regions are simultaneously formed by successive use of the through-oxide ion-implantation technique. These n^+ layers contribute to the reduction of the parasitic resistance between the gate and the source, resulting in a high transconductance, 180 mS/mm, and a high gain, 8 dB, for X-band.

An undoped LEC GaAs substrate was used. The dose condition adopted was 1×10^{13} cm^{-2} dose at 70 keV and 5×10^{13} cm^{-2} dose at 140 keV for the n^- and n^+ layers, respectively. The wafers were annealed at 830°C for 15 min in an N_2 atmosphere without any cap material. Au/Ni/AuGe and Al/Ti layers were used for the ohmic contacts and the Schottky gate, respectively. These metal patterns were formed by a lift-off process. The microstrip lines were composed of selective Au plated lines. The capacitors were of the MIM type, where the dielectric material was a plasma-CVD silicon nitride thin film.

A photograph of the chip of the analog frequency divider with a 500-μm gate width buffer amplifier is shown in Fig. 8. The chip size is 1.2 mm × 1.4 mm.

IV. EXPERIMENTAL RESULTS

The input threshold power is plotted as a function of input frequency in Fig. 9. No additional matching circuit is used for 50-Ω measurement systems. The bias voltages of V_{d1}, V_{g1}, and V_{g2} are 8 V, −0.71 V, and −0.80 V, respectively. The drain bias voltage of V_{d2} and the gate bias voltage of V_{g3} for the buffer amplifier are 8 V and −0.68 V, respectively. The minimum input threshold power is as low as 1.4 dBm at an input frequency of 14.7 GHz. The operation frequency band ranges from 14.2 to 15.3 GHz. It is considered that this operation bandwidth is determined not by the delay times of the FET and microstrip lines, but by the Q value of the feedback circuit. The center input frequency of 14.7 GHz is higher than the designed center frequency of 14.0 GHz because the coupling effect of the microstrip lines is stronger than the design estimation.

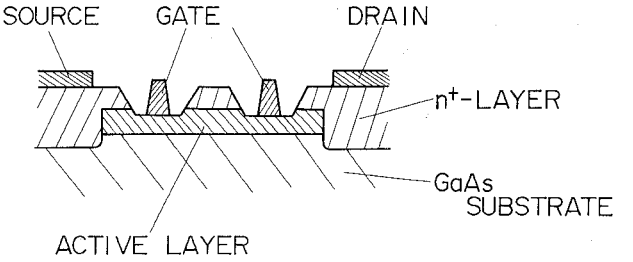

Fig. 7. Cross-sectional drawing of the dual-gate FET.

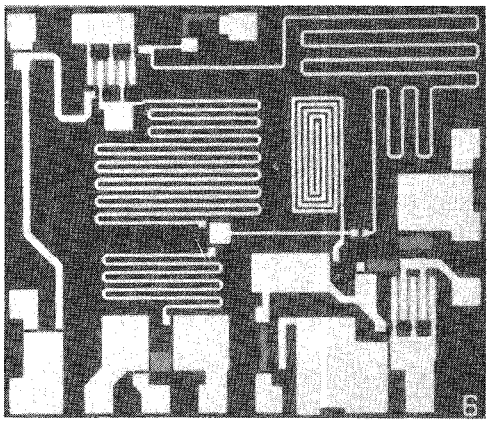

Fig. 8. Photograph of the 15 GHz single-stage GaAs dual-gate FET monolithic analog frequency divider with a buffer amplifier.

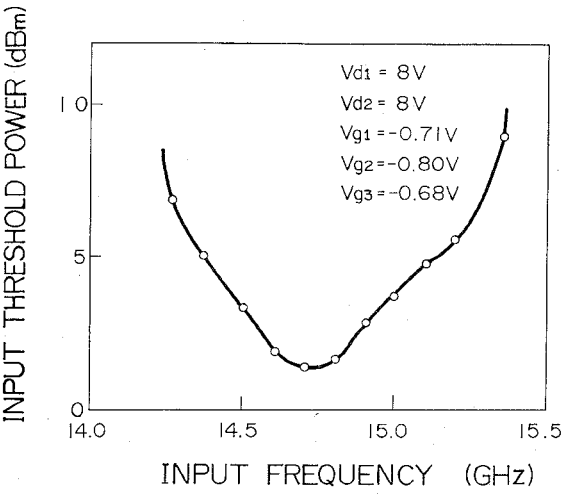

Fig. 9. Measured input threshold power as a function of input frequency.

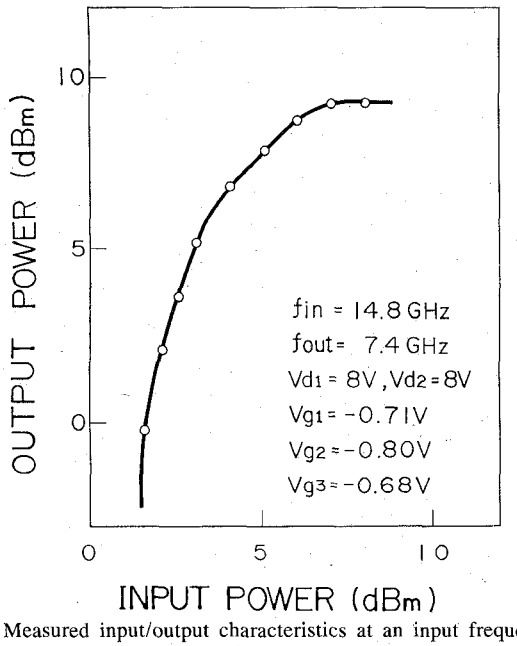

Fig. 10. Measured input/output characteristics at an input frequency of 14.8 GHz.

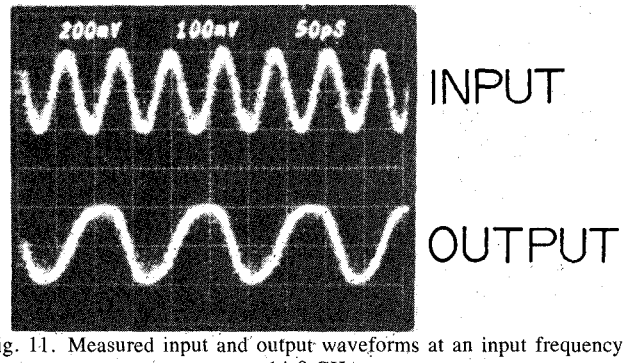

Fig. 11. Measured input and output waveforms at an input frequency of 14.8 GHz.

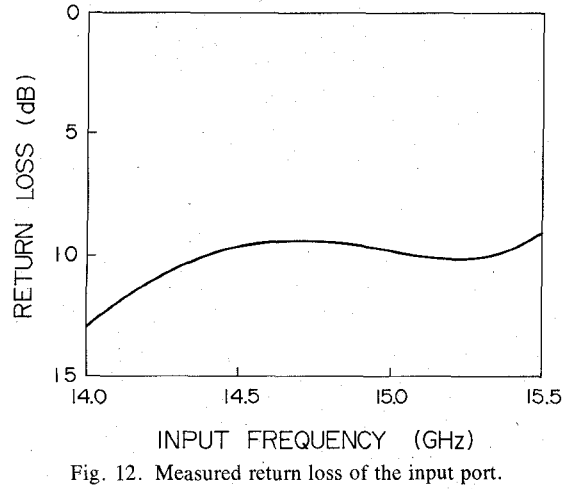

Fig. 12. Measured return loss of the input port.

The input/output characteristics at 14.8 GHz are shown in Fig. 10. The high conversion gain of 0.0–2.5 dB is obtained for an input power of 2.0–9.5 dBm. The output power is saturated at the input drive level over 7 dBm.

The input and output waveforms observed are shown in Fig. 11. The input and output frequencies are 14.8 and 7.4 GHz, respectively. The simple sinusoidal output waveform obtained is due to the fact that the signal of the input frequency is efficiently suppressed at the output port. The input frequency signal power taken out at the output port is −14.3 dBm for an input power of 3 dBm. The high input/output separation of signals attained is due to the good design of the rejection filter.

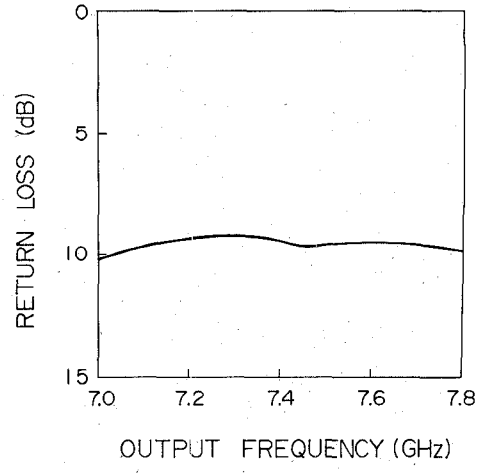

Fig. 13. Measured return loss of the output port.

The return loss of the input port is shown in Fig. 12. The return loss of 9.6–11.3 dB is obtained over the frequency range from 14.2 to 15.3 GHz.

Fig. 13 shows the return loss versus frequency characteristics at the output port. The return loss of 9.3–9.7 dB is obtained over the frequency range from 7.1 to 7.6 GHz.

V. Conclusion

A 15-GHz single-stage GaAs dual-gate FET monolithic analog frequency divider with a reduced input threshold power has been designed and fabricated. Use of the dual-gate FET and of the rejection filter has contributed to a simplification of the circuit configuration and a reduction of the input threshold power, respectively. This analog frequency divider MMIC has exhibited an input threshold power of 1.4 dBm in the operation frequency band from 14.2 to 15.3 GHz. This proposed divider circuit promises to be very valuable to the development of monolithic PLL's.

Acknowledgment

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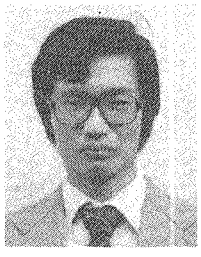

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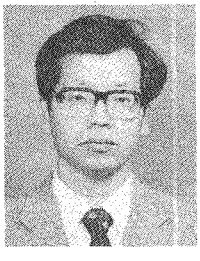

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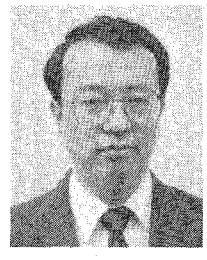

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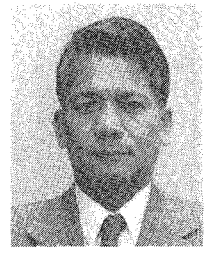

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